

## SYMMETRICAL HIGH FREQUENCY SCR STRUCTURE AND METHOD

## Background of the Invention

5   **[0001]**     This invention relates, in general, to integrated circuit structures, and more particularly to a low trigger voltage symmetrical SCR structure for protecting high frequency integrated circuits from electro-static discharges (ESD).

10   **[0002]**     High frequency (1 GHz and greater) integrated circuits are well known and used, for example, in personal communication applications such as cellular telephones, pagers, and personal digital assistant (PDA) devices. As the personal communications industry is  
15 pushed towards smaller and lighter products, the components and chips that make up these products must also become smaller and lighter.

**[0003]**     ESD is a well-known and documented problem in integrated circuit (IC) manufacturing. ESD occurs when  
20 large voltage pulses from static electricity are applied to the pads of integrated circuits. ESD voltage spikes may cause damage to insulating layers and conductive interconnects, which can result in short and/or open circuit failures and overheating. Additionally, such  
25 spikes can damage the junctions causing cross diffusion and melting.

**[0004]**     ESD protection has emerged as a major design challenge in high frequency applications such as radio frequency (RF) integrated circuits. In RF IC  
30 applications, higher failure voltages and smaller available areas for placing an ESD structure on an IC are driving factors for ESD performance levels.

**[0005]**     Additionally, an ESD load often dominates the parasitic capacitance (typically in the range of 1-8 pF),  
35 which becomes a significant problem at operating frequencies around 1 to 2 GHz. ESD device parasitic capacitance slows signals down, causes large reflections, and limits chip-to-chip signal bandwidth. As a result, a significant part of a signal is lost through ESD

circuits, which makes them a major obstacle for high-speed operation.

5     **[0006]**     In narrowband IC designs, it is known in the prior art to use a package/bond wire inductance technique to resonate out parasitic capacitance. However, this approach is not applicable to broadband designs, and thus, ESD parasitic capacitance continues to be a major problem in broadband applications. High frequency devices such as RF IC's often do not include ESD structures because of the capacitive loading problem, and are thus, very susceptible to damage and/or failure.

10    **[0007]**     Accordingly, a need exists for a low voltage ESD structure having an acceptable capacitive load (i.e., less than about 0.1 to 0.2 pF) for high frequency applications (i.e., 1 GHz to 10 GHz). Further, it would be beneficial for the ESD structure not to consume too much chip real estate, and to be easily integrated into a chip fabrication process.

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#### Brief Description of the Drawings

25    **[0008]**     FIG. 1 is a circuit diagram of a prior art input ESD structure;

30    **[0009]**     FIG. 2 is a circuit diagram of a prior art output ESD structure;

**[0010]**     FIG. 3 is simplified equivalent capacitance circuit including the ESD structure of FIG. 1;

**[0011]**     FIG. 4 illustrates an enlarged cross-sectional view of a prior SCR ESD structure;

**[0012]**     FIG. 5 illustrates an enlarged cross-sectional view of an SCR structure according to the present invention;

**[0013]**     FIG. 6 illustrates an enlarged cross-sectional view of another portion of the structure of FIG. 5;

35    **[0014]**     FIG. 7 is a graph of transmission line pulse current versus ESD stress voltage comparing the SCR structure of FIG. 5 to the prior art ESD structure of FIG. 1;

[0015] FIG. 8 is a graph of capacitance versus voltage comparing the SCR structure of FIG. 5 to the prior art diode structure of FIG. 1;

5 [0016] FIG. 9 is a circuit diagram of a high frequency integrated circuit structure including an SCR structure according to the present invention; and

[0017] FIG. 10 is a graph of a transient current/voltage (I-V) characteristic of an SCR structure according to the present invention.

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#### Detailed Description of the Drawings

[0018] In general, the present invention provides an  
15 SCR device suitable for high frequency (greater than 1 GHz) ESD protection. The SCR device comprises a symmetrical low trigger voltage r structure. In a preferred embodiment, the structure is integrated into a high frequency bipolar IC process flow, and is isolated  
20 from the internal circuitry it protects with a deep isolation trench structure, field dielectrics, and low-doped regions and layers. One can better understand the present invention by referring to FIGS. 1-10 together with the following detailed description of the drawings.

25 [0019] FIG. 1 is a simplified circuit diagram of a prior art high frequency input ESD structure 1. ESD structure 1 protects input pad 2 with two reverse biased Zener diodes 6 and 7, where Zener diode 6 is coupled from signal to a  $V_{CC}$  bus 8, and Zener diode 7 is coupled from  
30 signal to a  $V_{EE}$  bus 9. Additionally, a series resistor 3 (approximately 100 ohms) is coupled to input pad 2, Zener diodes 6 and 7, and internal circuitry 11. Zener diode 12 is coupled to  $V_{CC}$  bus 8 and  $V_{EE}$  bus 9 and provides a power clamp or central protection device for internal  
35 circuitry 11.

[0020] FIG. 2 is a simplified circuit diagram of a prior art high frequency output ESD structure 14. ESD structure 14 protects an output pad 16 with two reverse biased Zener diodes 17 and 18, where Zener diode 17 is

coupled from signal to  $V_{CC}$  bus 8, and Zener diode 18 is coupled from signal to  $V_{EE}$  bus 9. Zener diodes 6, 7, 12, 17 and 18 have a breakdown voltage of about 7 volts. Zener diode 12 typically is twice the area of Zener diodes 6, 7, 17 and 18.

**[0021]** FIG. 3 shows an equivalent capacitance circuit 21 of an ESD protection structure including ESD structure 1 where load capacitances of protected internal circuitry are ignored. The parasitic capacitance of a given input/output pad can be estimated by the following formula:

$$C_{\text{Pad}/V_{CC}} = C_{\text{Pad}/V_{EE}} = [(m+1)C_P + 2C_C] / [1 + (m/2) + (C_C/C_P)] \quad (1)$$

In the above formula,  $m=n-1$ ,  $C_P$  is the capacitance of an ESD protection device (e.g., Zener diodes 6, 7, 17, and 18),  $C_C$  is the capacitance of a central protection ESD device (e.g., Zener diode 12), and  $n$  is the number of input/output pads in a given circuit. As can be seen from the formula, the parasitic input/output capacitance of a given  $C_{\text{pad}/V_{CC}}$  tends to  $2C_P$ , and does not depend on the central protection device capacitance  $C_C$  or the number of pads  $n$ .

**[0022]** In the ESD structures of FIG. 1 and FIG. 2, the capacitance of a Zener diode (e.g., diodes 6, 7, 17 and 18) alone is on the order of 0.9 pF, and the parasitic capacitance load at a given pad ( $C_{\text{pad}/V_{CC}}$ ) is greater than 1.8 pF. This value of parasitic capacitance becomes a significant problem for RF applications because, among other things, it limits chip-to-chip bandwidth and causes signal loss through the ESD structure.

**[0023]** Additionally, bias dependant diode junction capacitance is an issue with ESD structure 1 because the input capacitance varies when an input signal has different voltage levels. This can cause a threefold degradation in signal quality for a voltage swing of 0 to  $V_{CC}$  (i.e., 5 volts). For high precision circuit operations, an input capacitance of an analog pin must be

kept as constant as possible within an input voltage swing. The input capacitance variation of ESD structure 1 causes an increase in harmonic distortion in analog-to-digital converter applications, and thus, degrades the precision of the device.

**[0024]** SCR devices have been proposed as ESD devices in CMOS integrated circuits. SCR devices have several advantages including their high energy absorbing capability and their small size (i.e., they take up less space on chip compared to conventional devices such as ESD structure 1). Additionally, SCR's have low dynamic on-resistance and low power dissipation compared to diodes, MOS transistors, and bipolar transistors.

**[0025]** However, unless certain precautions are taken, SCR devices also have several disadvantages. FIG. 4 shows a cross-sectional view of a prior art CMOS based SCR ESD device 21, which is used to illustrate such disadvantages. Device 21 includes a p-type substrate 22, an n-well 23, and a p-well 24 in contact with n-well 23. Device 21 further includes n+ regions 26 and 27, and p+ regions 28 and 29. A contact 31 couples n+ region 26, n-well 23, and p+ region 28, and a contact 32 couples n+ region 27, p-well 24, and p+ region 29.

**[0026]** SCR device 21 has a relatively high trigger voltage  $V_t$  on the order of 20 to 25 volts because of low-doped n-well 23 and p-well 24, which typically having doping levels on the order of  $1.0 \times 10^{17}$  atoms/cm<sup>3</sup>. This becomes a problem as IC geometries shrink below 0.8 microns because gate oxide failure voltages become close to the lowest junction breakdown voltage of typical SCR devices. At the 0.8 micron level, worst case gate oxide breakdowns occur in the 10 to 12 volt range, and naturally triggered or typical SCR devices like device 21 require about a 20 to 25 volt transient to turn on. Such a trigger voltage is too high to protect current and future device geometries.

**[0027]** Another disadvantage of SCR device 21 is its tendency to remain in an "on" state because of parasitic

triggering in normal operations from effects such as noise, fast pulse rates, or the like. Also, if circuit connections to SCR device 21 are capable of supplying current in excess of the SCR's holding current, it remains in a conductive, clamped state when a transient is finished. This can produce catastrophic results on an ESD device or an IC structure the ESD device is supposed to protect. As a result of these disadvantages, SCR device 21 cannot be used by itself to protect I/O pads.

**[0028]** Several modifications and solutions have been proposed to overcome the deficiencies of SCR device 21. For example, an additional n+ or p+ region is placed between n-well 23 and p-well 24 to reduce the breakdown voltage, which in turn, reduces the trigger voltage. Alternatively, a gate grounded NMOS transistor or PMOS transistor is added to reduce the breakdown voltage between n-well 23 and p-well 24.

**[0029]** In addition, control circuits that include series diodes and MOS transistors have proposed to increase holding voltage over a particular supply bias. Also, control circuits including diodes and grounded gate MOS transistors have been proposed to increase holding current over a particular operating current. Key disadvantages of these proposed solutions include a larger required area on the chip for ESD structure integration, and an increase in the ESD structure's load capacitance, which is directly contrary to the high frequency IC design requirements set forth above.

**[0030]** Turning now to the present invention, the authors propose a symmetrical silicon controlled rectifier (SCR) structure to solve the problems and challenges set forth in prior art. The proposed structure is symmetrical in order to, among other things, protect for positive and negative HBM ESD stress.

**[0031]** FIGS. 5-10 show a preferred embodiment of an SCR structure suitable for ESD protection in high frequency IC applications. The key advantages of the device according to the present invention are its reduced

trigger voltage, low capacitance, ability to outperform prior art configurations, and its small size.

Additionally, the SCR device according to the present invention is conveniently implemented in a standard high  
5 frequency bipolar flow thereby minimizing any impact of ESD device integration. The dopant profiles described in a preferred embodiment provide an SCR device that has a trigger voltage on the order of 9 to 10 volts, and a clamping voltage on the order of 6 to 7 volts. The  
10 profiles are adjusted to provide other desired trigger and clamping voltage characteristics.

**[0032]** FIG. 5 illustrates an enlarged cross-sectional view of an SCR structure or device 41 in accordance with the present invention. SCR structure 41 is designed, for  
15 example, as an ESD structure for protecting I/O pads and power rails with a reduced load capacitance for high frequency applications. Additionally, SCR structure 41 is designed to provide a flatter capacitance-voltage (C-V) characteristic.

**[0033]** SCR structure 41 comprises symmetrical p-n-p-n SCR devices, and includes a p+ semiconductor wafer or layer 417 having a preferred dopant concentration on the order of  $4.0 \times 10^{17}$  to  $6.0 \times 10^{17}$  atoms/cm<sup>3</sup>, a lightly doped p-layer or region 416 on or over p+ layer 417, an n+ buried  
25 layer or region 413 on or over p- layer 416, and n- layer or region 414 formed on or over n+ buried layer 413. Together, p+ layer 417, p- layer 416, buried layer 413, and n- layer 414 form a semiconductor substrate or body of semiconductor material 43.

**[0034]** According to the present invention, n+ buried layer 413 is maintained floating (i.e., not directly couple to a power rail or ground) to ensure a symmetrical DC breakdown voltage response, and to decrease load capacitance. In addition, n+ buried layer 413 reduces by  
35 approximately half the maximum transient voltage bias clamp that results from an ESD event. This allows a very fast and efficient ESD protection, and further reduces required ESD device area on a chip.

- [0035]** Preferably, p- layer 416 has a dopant concentration of about  $1.0 \times 10^{13}$  atoms/cm<sup>3</sup> and a thickness of about 1.5 to 3.0 microns. N+ buried layer 413 has a dopant concentration of about  $8.0 \times 10^{19}$  atoms/cm<sup>3</sup> and a thickness of about 0.75 to 1.75 microns. N- layer 414 has a dopant concentration of about  $2.0 \times 10^{16}$  atoms/cm<sup>3</sup> and a thickness of about 0.8 to 1.2 microns. P- layer 416 is formed using conventional epitaxial growth techniques. N+ buried layer 413 is formed using conventional masking, deposition, and doping/diffusion techniques, or alternatively, with epitaxial growth techniques. N- layer 414 is formed using, for example, conventional epitaxial growth techniques.
- [0036]** A first p- well 411 and a second p- well 421 are formed within n- layer 414, and are spaced apart leaving a portion of n- layer 414 between the two p- wells. Preferably, p- wells 411 and 421 are spaced a distance of about 3.0 to about 4.0 microns apart. P- wells 411 and 421 preferably have a peak concentration on the order of  $3.0 \times 10^{18}$  atoms/cm<sup>3</sup> and are diffused to a depth to contact n+ buried layer 413 (about 0.9 to about 1.2 microns). P- wells 411 and 421 are formed using conventional masking, doping and diffusion techniques, and preferably are formed at the same time.
- [0037]** A deep isolation trench 419 separates or isolates SCR structure 41 from the internal circuitry it protects. Deep isolation trench 419 extends from a surface 42 of SCR structure 41 into p+ layer 417, and is filled with a deposited dielectric 427 such as a deposited oxide (e.g., a tetraethylorthosilicate (TEOS) oxide) and a floating doped polycrystalline silicon layer 426 (e.g., p+ doped polysilicon). Deep isolation trench 419 preferably is capped with a field dielectric layer 428.
- [0038]** A field dielectric layer 418 separates p- wells 411 and 421, and has a thickness on the order of 0.6 microns. Field dielectric layers 418 and 428 comprise a silicon oxide for example, and are formed using



conventional masking and oxide growth techniques (e.g., LOCOS isolation techniques). Field dielectric layer 418 together with a portion of n- layer 414 isolates first p-well 411 and second p- well 421. Additionally, the deep  
5 isolation trenches and field dielectric layers form a plurality of active regions on semiconductor substrate 43 where ESD structures (e.g., SCR structure 41) and other circuitry (e.g., internal circuitry 53 shown in FIG. 9) are formed.

10 **[0039]** N+ regions or doped regions 412 and 422 are formed in first p- well 411 and second p- well 421 respectively. P+ regions or doped regions 415 and 425 are formed in first p- well 411 and second p- well 421 respectively, and are spaced apart from n+ regions 412  
15 and 422. Preferably, n+ regions 412 and 422 are formed at the same time, and p+ regions 415 and 425 are formed at the same time. A first ohmic contact 431 is formed over n+ region 422 and p+ region 425 thereby electrically coupling regions 422 and 425, and second ohmic contact  
20 433 is formed over n+ region 412 and p+ region 415 thereby electrically coupling regions 412 and 415.

**[0040]** P+ regions 415 and 425 have a surface concentration of about  $2.0 \times 10^{20}$  atoms/cm<sup>3</sup> and a depth of about 0.2 to about 0.3 microns. N+ regions 412 and 422  
25 have a surface concentration of about  $1.0 \times 10^{21}$  atoms/cm<sup>3</sup> and a depth of about 0.1 to about 0.2 microns. By way of example, p- well 411, p+ region 415, n+ region 412, and ohmic contact 433 form an anode of SCR structure 41, and p-well 421, p+ region 425, n+ region 422, and ohmic  
30 contact 431 form a cathode of SCR structure 41.

According to the present invention, the built-in resistances of p-wells 411 and 421 and n+ buried layer 413 ensure a relatively high holding voltage ( $V_h$ ), which allows SCR device 41 to overcome the tendency of  
35 conventional SCR devices to remain in a clamped "on" state when parasitic triggering events occur.

**[0041]** SCR structure 41 is symmetrical about axis 409, which bisects p- well 411, with only half of it shown in

FIG. 5. The anode and cathode sides of the device are junction isolated with n- layer 414, which is also isolated from the top with field dielectric layer 418. SCR structure 41 is further junction isolated from p+ substrate 417 with low-doped p- layer 416, which ensures a very low capacitance 444. Additionally, deep trench 419 provides a low capacitance (i.e., capacitances 445 and 446) lateral isolation of SCR structure 41 from the protected internal circuitry (shown in FIG. 9).

Parasitic capacitances 443 and 444 are parallel to main device capacitances 441 connected in series. Capacitances 445 and 446 are serial and paralleled to a lower part of the circuit (i.e., cathode side).

**[0042]** The equivalent capacitance circuit of SCR device 41 ensures a very flat capacitance voltage characteristic (shown in FIG. 8), which provides a significant improvement over the prior art. The overall reduction in capacitance of SCR structure 41 is due to its smaller junction area and the series connected capacitances 441 of the p-n junctions between layers 411/413 and 421/413. Additionally, the flatness of the C-V characteristic results from the series capacitances of SCR structure 41. For example, during a positive bias, one junction becomes depleted causing its capacitance to decrease because of an increase in space charge width. The other junction remains unchanged, and thus, its capacitance is kept quasi-constant. Thus, the decrease in capacitance of SCR structure 41 capacitance is less compared to ESD structure 1, which is a one junction device. A negative bias alters the role of the polarized junctions, but the overall SCR capacitance retains a tendency to decrease slightly. In comparison, diode junction in ESD structure 1 becomes accumulated, which causes its space charge width to decrease. This results in a strong increase in capacitance.

**[0043]** FIG. 6 illustrates an enlarged cross-sectional view of another portion of SCR structure 41. P+ layer 417 preferably is coupled to the  $V_{EE}$  bus via a deep

contact trench 439. Deep contact trench 439 is filled with a polycrystalline silicon layer 426 (e.g., p+ doped polysilicon).

5     **[0044]**     As shown in FIG. 5, the cathode and anode sides of SCR structure 41 are physically symmetrical low-voltage p-n-p-n thyristors in terms of device DC current-voltage characteristics and ESD operation. That is, the two SCR devices have symmetrical IV characteristics in DC and transients modes of operation. Regions and layers  
10    415, 411, 413, 421 and 422 form one p-n-p-n device, and regions and layers 425, 421, 413, 411 and 412 form a second p-n-p-n device.

15     **[0045]**     SCR structure 41 has excellent isolation properties. Using trench isolation (e.g., deep isolation trench 419), which surrounds SCR structure 41, leakage current levels are negligible. This reduces any probability of latch-up into internal circuitry that is near SCR structure 41 (shown as internal circuitry 53 in FIG. 9). Additionally, high-doped p+ layer 417 and the  
20    deep p+ doped polysilicon filled deep trench substrate contact to  $V_{EE}$  or ground provide an efficient barrier to reduce any substrate current injection and cross-talk mechanisms with adjacent internal circuitry.

25     **[0046]**     The following table summarizes a comparison of device performance between ESD structure 1 (prior art) and SCR structure 41:

Device	BV	ESD Stress	V <sub>tr</sub>	Min V <sub>h</sub>	C-V Swing C <sub>max</sub> /C <sub>min</sub>	C <sub>load</sub> @0V	Efficiency C <sub>diode</sub> /C <sub>load</sub>	Area $\mu\text{m}^2$
1	7.8V	2kV	7.5V		2.19	0.88 pF	1	1064
41	8V	3.25kV	8.8V	5.5V	1.23	0.28 pF	2.5-4.28 flat	640

Where, BV is DC breakdown voltage, V<sub>tr</sub> is the trigger voltage (shown in FIG. 10 as point 61 on the IV curve),  
 5 Min V<sub>h</sub> is the minimum holding voltage (shown in FIG. 10 as point 62 on the IV curve), C-V Swing is a ratio of maximum to minimum capacitance, C<sub>load</sub> is the load capacitance of the ESD device, Efficiency is normalized with respect to ESD device 1, and Area includes total  
 10 area of the ESD device without pads.

**[0047]** FIG. 7 is a graph of transmission line pulse (TLP) current versus voltage comparing SCR structure 41 (line 206) to ESD structure 1 (line 207). As shown in FIG. 7, SCR device 41 shows a maximum TLP bias voltage of  
 15 11 volts at 1 amp, while ESD device 1 shows a maximum TLP bias voltage of 24 volts at 1 amp. FIG. 8 is a graph that shows a capacitance versus voltage bias comparison between ESD structure 1 (line 208) and SCR structure 41 (line 209). In both FIG. 7 and 8, the device area of ESD  
 20 structure 1 is 1064  $\mu\text{m}^2$ , and the device area of SCR structure 41 is 640  $\mu\text{m}^2$ .

**[0048]** FIGS. 7 and 8 together with the above Table illustrate the enhanced performance of SCR structure 41 compared to prior art high frequency ESD structure 1.  
 25 SCR structure 41 shows an improved robustness in terms of sustained ESD threshold voltage stress. In addition, the device capacitance is approximately half. Also, the input capacitance of SCR structure 41 remains almost constant, even when input voltage swings from 0 to V<sub>cc</sub>  
 30 (5V). Additionally, the device area of SCR structure 41 is approximately 60% that of ESD structure 1.

**[0049]** FIG. 9 shows an equivalent circuit of a high frequency integrated circuit device 51 that includes I/O ESD protection circuit 510, I/O pad 514,  $V_{EE}$  or ground bus 517, and internal circuitry 53. ESD protection circuit 510 includes two symmetrical low voltage trigger SCR (SLVTSCR) devices according to the present invention. Circuit 510 is coupled to an I/O pad 514 and a  $V_{EE}$  bus 517. Although not shown, in a full implementation, a second ESD protection circuit similar to 510 is coupled to I/O pad 514 and a  $V_{CC}$  bus or power rail. Internal circuitry 53 comprises for example, bipolar power amplifier devices, logic devices, interstage matching network devices, and/or the like.

**[0050]** ESD protection circuit 510, I/O pad 514,  $V_{EE}$  bus 517, and internal circuitry are formed on a semiconductor substrate, such as substrate 43 shown in FIG. 5, where the term "on" means the structures are within substrate 43, over substrate 43 (such as overlying isolation regions), and/or contacting upper surface 42 of substrate 43.

**[0051]** Referring back to FIG. 5, n+ region 412, p-region 411 and n+ buried layer 413 form respectively an emitter, base and collector of n-p-n vertical transistor 110 (shown in FIG. 9). N+ region 422, p-region 421, and n+ buried layer 413, form respectively, an emitter, base, and collector of symmetrical n-p-n vertical transistor 120. N+ buried layer 413 and n- layer 414 form an n-type base, and p+ regions 415 and 425 form respectively, the emitter/collector regions of p-n-p lateral bipolar transistor 113. Resistors 112 and 122 are formed, respectively, from the distributed resistance of p-regions 411 and 421.

**[0052]** Resistors 111 and 121 are formed, respectively, from the distributed resistance of n+ buried layer 413 and n- layer 414. Vertical p-n-p transistor 114 is formed from p+ substrate 417 (emitter/collector), n+ buried layer 413 (base) and p- regions 415/411 (collector/emitter), where resistor 115 is the

distributed resistance of p+ substrate 417. Second vertical p-n-p transistor 124 is formed from p+ substrate 417 (emitter/collector), n+ buried layer 413 (base) and p- layers 425/421 (collector/emitter).

5   **[0053]**     Structure 510 forms a functional circuit block with two terminals, working in combination separately, i.e., devices 110, 114, and 113 in one direction, and 120, 124, and 113 in the opposite direction, respectively, to protect internal circuitry 53 against  
10   ESD stress. The DC breakdown voltages of the base/collector and/or base/emitter junctions of p-n-p devices 113 are about 7 volts. Under normal conditions (i.e., operation voltage <  $V_{CC}$ ), ESD device 51 is off with only negligible leakage currents flowing in the circuit.

15   **[0054]**     By way of example, consider a mode where I/O pad 514 is connected to the anode, and  $V_{EE}$  bus 517 is coupled to the cathode. If a positive ESD stress is considered at I/O pad 514 with respect to  $V_{EE}$ , the p-n junction formed between regions 411 and 413 is forward  
20   biased, and the p-n junction between regions 421 and 413 is reverse biased. At the same time, the p-n junction between layers 413 and 416 becomes reverse biased. The latter p-n junction has a very high breakdown voltage (>50 volts) because of low-doped p-layer 416.

25   **[0055]**     When the reverse bias exceeds the avalanche breakdown of the p-n junction formed by p- well 421 and n+ buried layer 413 (around 7 volts DC), the current through transistor 113 increases and additional carriers (electron-hole pairs) are generated. The generated holes  
30   accelerate in p- well 421 and p+ region 425, and are collected by ohmic contact 431 (i.e., the cathode). Because of hole drift along these p doped regions, the voltage drop across resistor 122 increases.

35   **[0056]**     When the voltage bias at the p-n junction between p- well 421 and n+ region 422 exceeds 0.6-0.7 volts, the base/emitter junction of n-p-n transistor 120 becomes forward biased and the SCR device turns on. As the collector current across resistor 121 increases, the

voltage drop at the base/collector of p-n-p transistor 113 decreases. As a result, the device is turned on and triggers into snap back. The device according to the present invention forms a very low impedance path between the electrodes, and the ESD induced current is evacuated into the protection circuit instead of internal circuitry 53. During a positive stress bias, transistor 124 is not turned on because the breakdown voltage of the reverse biased base/collector junction is very high. Thus, only a small amount of current flows through transistor 124.

**[0057]** FIG. 10 shows a transient I-V characteristic for an SCR device from ESD structure 51, which results from a transient bias. Point 61 on the IV curve represents the trigger voltage and current ( $V_{tr}$  and  $I_{tr}$ ), and point 62 represents the holding voltage and current ( $V_h$  and  $I_h$ ). Point 63 represents a maximum voltage above which failure of internal circuitry occurs. Region 64 represents a preferred I-V operation area, and region 66 represents an ESD design window. The characteristic for an negative stress is symmetrical according to the present invention to the one shown in FIG. 10.

**[0058]** The robustness of ESD structure 51 results from, among other things, two critical parameters: 1) a trigger voltage  $V_t$  of approximately 9 to 10 volts and a trigger current  $I_t$  of approximately 0.02 amps on one side of the device, and 2) a holding voltage  $V_h$  of about 6 to 7 volts and a holding current  $I_h$  of about 0.2 amps, on the other side of the device. When the voltage bias between electrodes increases beyond  $V_h$ , ESD structure 51 enters a snap back mode (i.e., it is turned on), and thus, a lower voltage is needed to sustain the current circulating across the device, corresponding to a negative resistance.

**[0059]** Beyond the holding voltage, a low-impedance mode of the device maintains a sharp I-V characteristic, and provides for low power dissipation in the device. This feature of the invention helps ESD structure 51 to sustain higher ESD threshold stress, and also is

responsible for the robustness of ESD protection circuit design. Additionally, ESD structure 51 has a fast response to ESD stress. The time from turn-off to turn-on (low impedance mode) takes about 1 nanosecond, and the design does not allow the device to overheat, which is a problem with the prior art.

**[0060]** Thus it is apparent that there has been provided, in accordance with the present invention, a symmetrical SCR protection device for high frequency ESD applications. The disclosed device has a low trigger voltage (i.e., 9-10 volts), low capacitance (less than 0.3 pF), outperforms prior art Zener diode configurations, and it has a small size. Because of its low capacitance, the SCR device according to the present invention reduces signal losses, does not cause large signal reflections, and does not limit chip-to-chip bandwidth. Additionally, the symmetrical SCR protection device is conveniently implemented in a standard high frequency bipolar integrated circuit process flow. Moreover, the SCR device according to the prevention is implemented without the additional diode or MOS transistor devices and control circuitry required by prior art SCR ESD structures.

**[0061]** Although the invention has been described and illustrated with reference to specific embodiments thereof, it is not intended that the invention be limited to these illustrative embodiments. Those skilled in the art will recognize that modifications and variations can be made without departing from the spirit of the invention. Therefore, it is intended that this invention encompass all such variations and modifications as fall within the scope of the appended claims.